

# MOS FIELD EFFECT TRANSISTOR

# 2SK2409

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK2409 is N-Channel MOS Field Effect Transistor designed for solenoid, motor, and lamp driver.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)} \leq 27 \text{ m}\Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ )  
 $R_{DS(on)} \leq 40 \text{ m}\Omega$  ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 20 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 2040 \text{ pF TYP.}$
- Built-in Gate Protection Diode

#### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Device" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

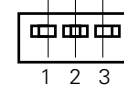
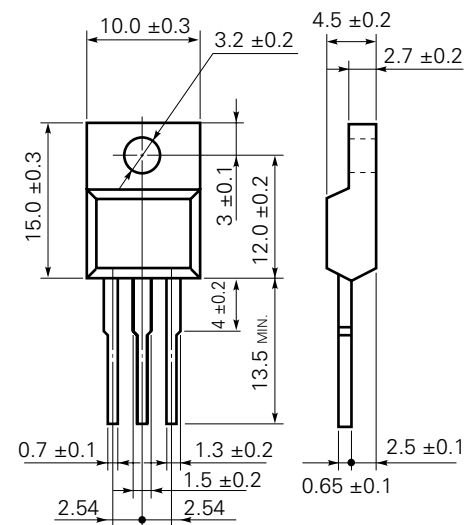
#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 40$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 160$	A
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	2.0	W
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	35	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current	$I_{AS}^{**}$	40	A
Single Avalanche Energy	$E_{AS}^{**}$	160	mJ

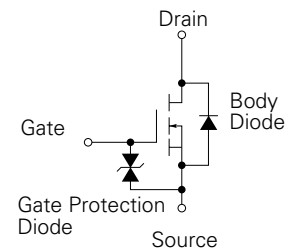
\*  $PW \leq 10 \text{ } \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ } \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

#### PACKAGE DIMENSION (in millimeters)



#### MP-45F (ISOLATED TO-220)



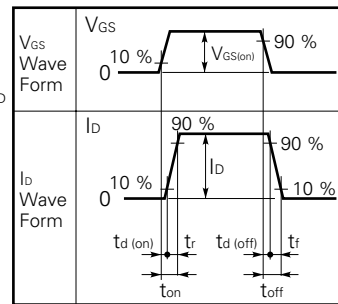
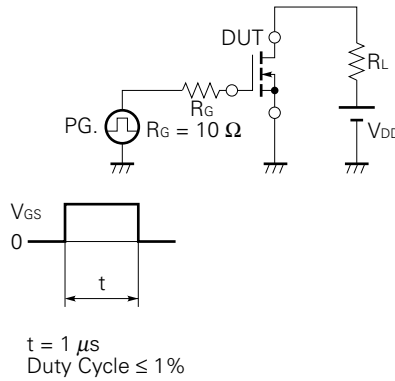
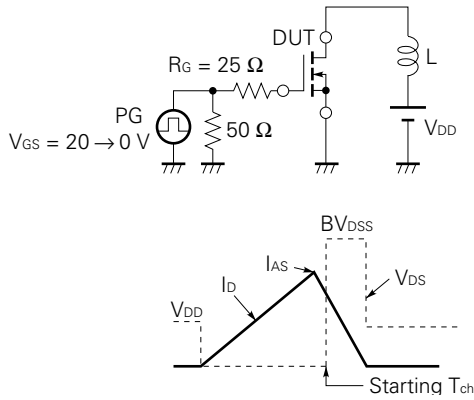
The information in this document is subject to change without notice.

**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

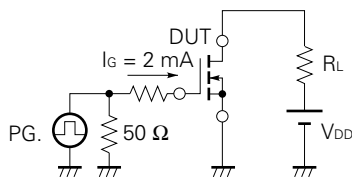
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>		22	27	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A
Drain to Source On-State Resistance	R <sub>DS(on)2</sub>		30	40	mΩ	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 20 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0	1.5	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	20	35		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A
Drain Cutoff Current	I <sub>bss</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2040		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		1080		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		300		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		30		ns	I <sub>D</sub> = 20 A
Rise Time	t <sub>r</sub>		350		ns	V <sub>GS(on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		210		ns	V <sub>DD</sub> = 30 V
Fall Time	t <sub>f</sub>		260		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		72		nC	I <sub>D</sub> = 40 A
Gate to Source Charge	Q <sub>GS</sub>		6.0		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		24		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		1.1		V	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		110		ns	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		360		nC	di/dt = 100 A/μs

**Test Circuit 1 Avalanche Capability**

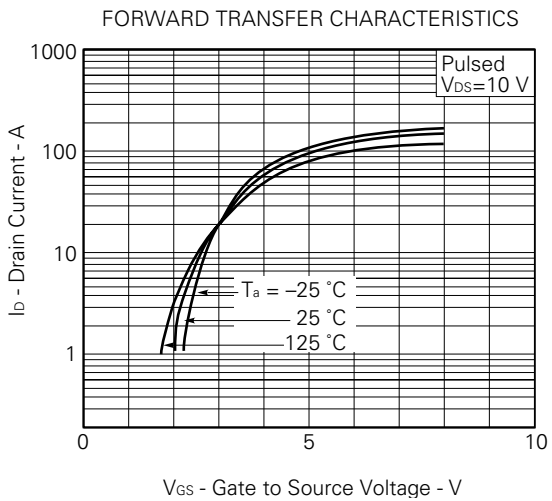
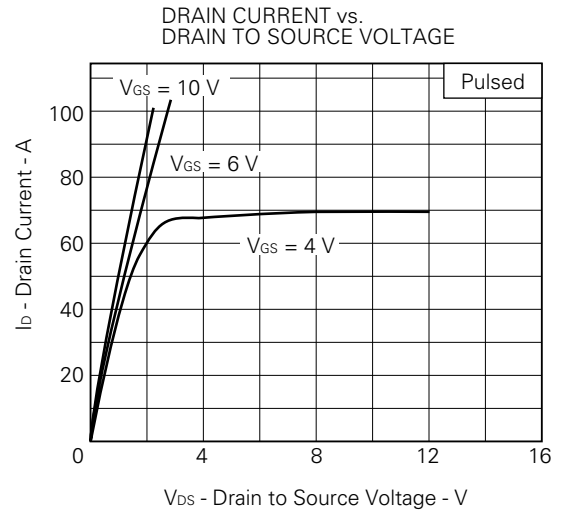
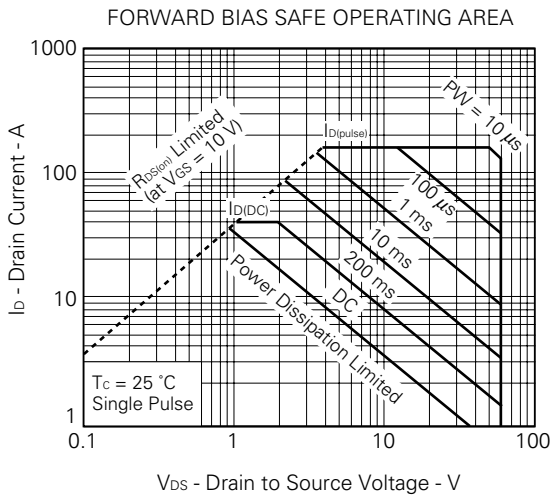
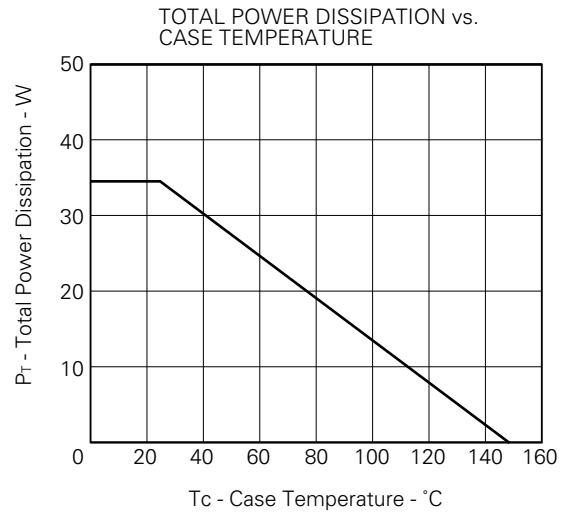
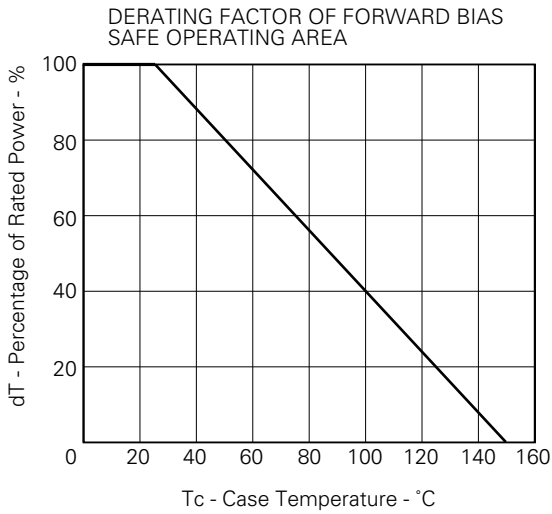
**Test Circuit 2 Switching Time**



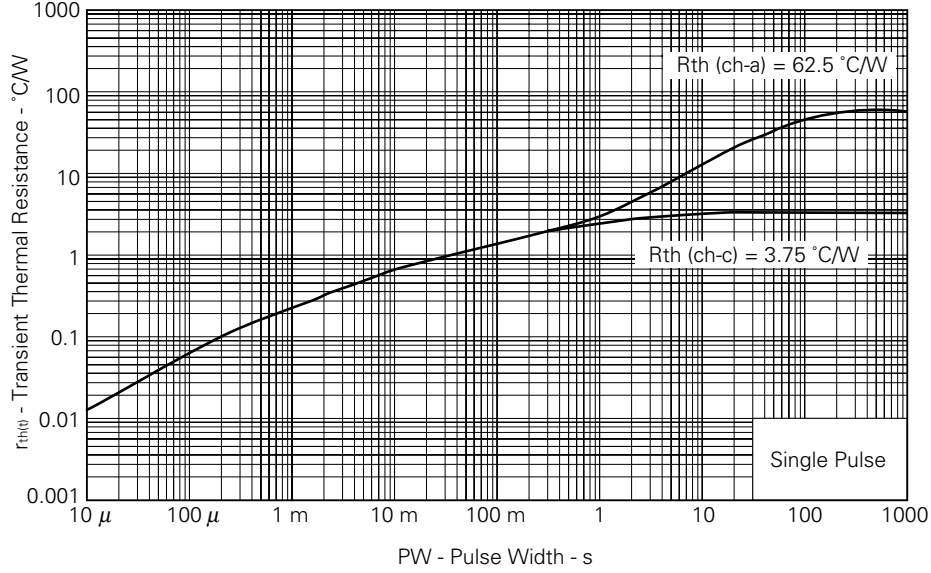
**Test Circuit 3 Gate Charge**



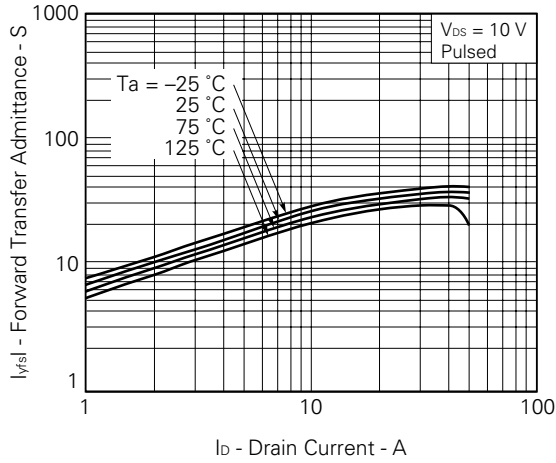
TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)



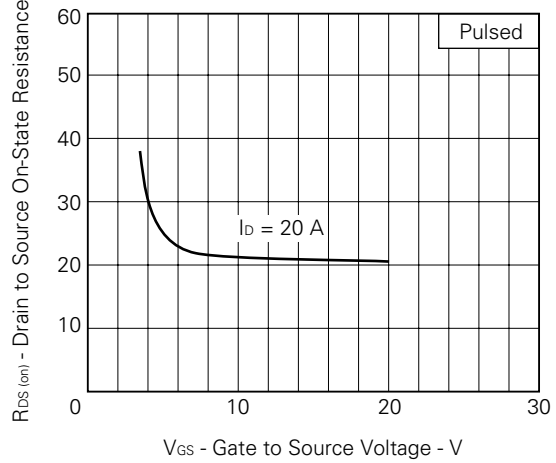
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



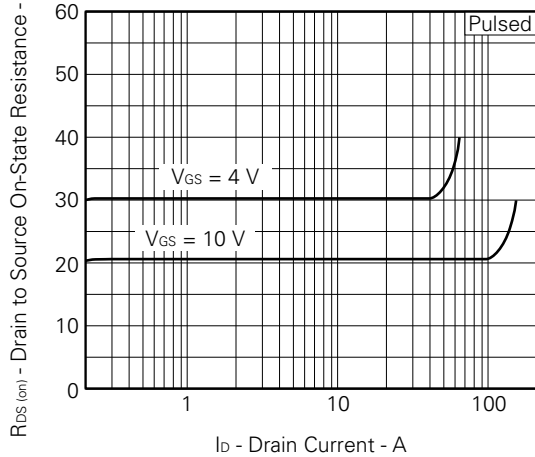
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



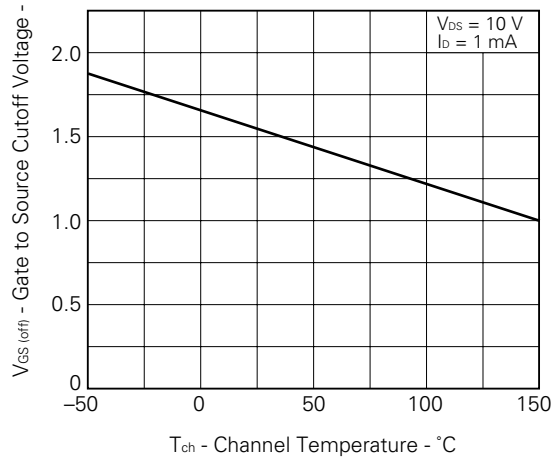
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

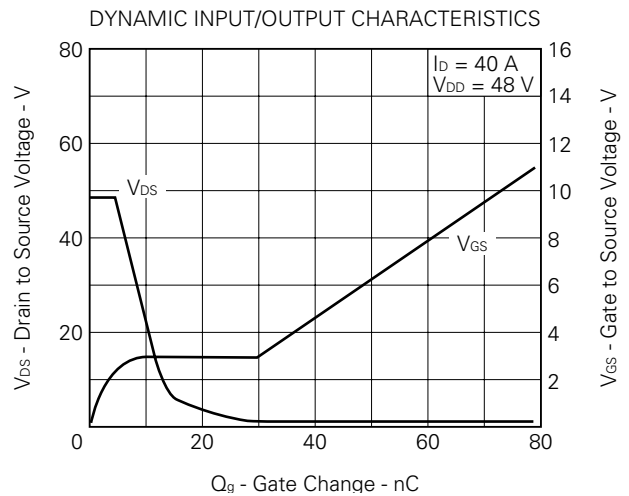
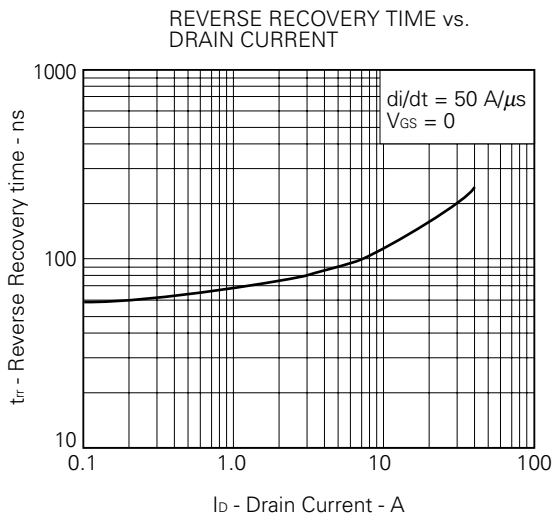
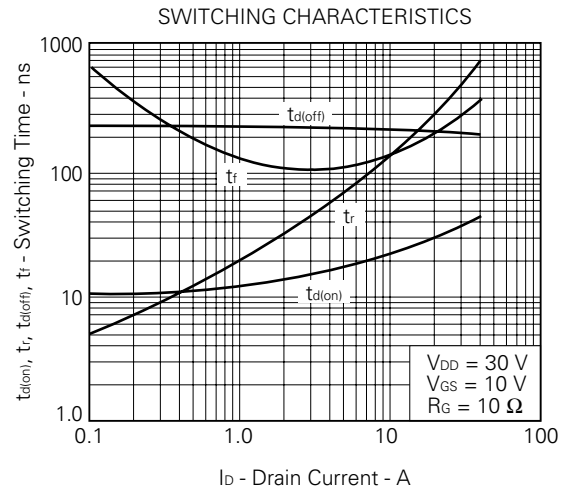
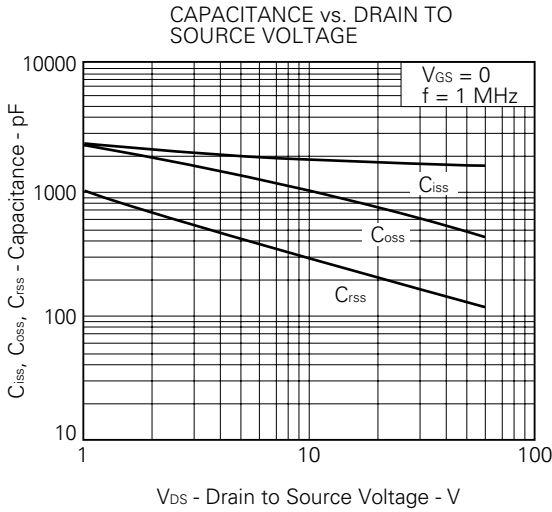
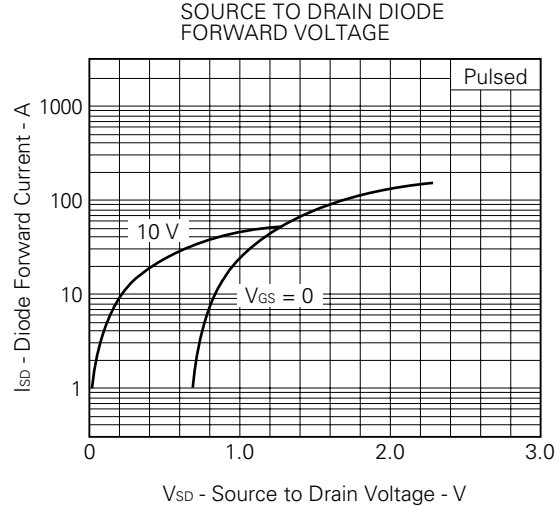
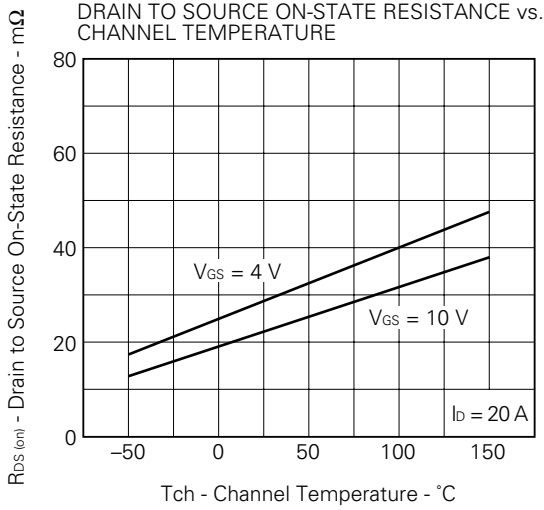


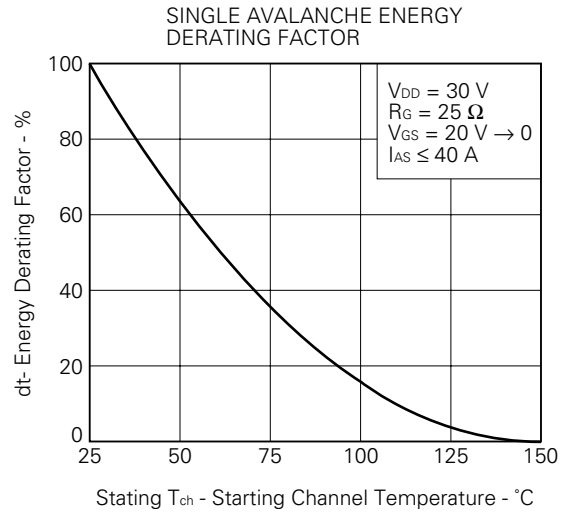
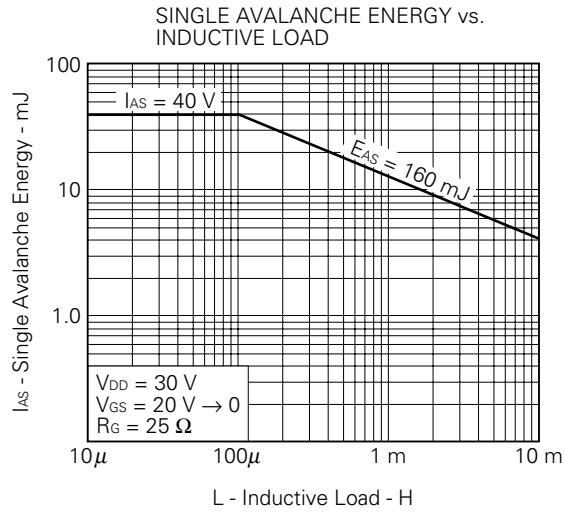
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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